Toward Minimum Graphic Parity Networks

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Abstract

Quantum circuits composed of CNOT and R_z are fundamental building blocks of many quantum algorithms, so optimizing the synthesis of such quantum circuits is crucial. We address this problem from a theoretical perspective by studying the graphic parity network synthesis problem. A graphic parity network for a graph G is a quantum circuit composed solely of CNOT gates where each edge of G is represented in the circuit, and the final state of the wires matches the original input. We aim to synthesize graphic parity networks with the minimum number of gates, specifically for quantum algorithms addressing combinatorial optimization problems with Ising formulations. We demonstrate that a graphic parity network for a connected graph with n vertices and m edges requires at least $m+n-1$ gates. This lower bound can be improved to $m+\Omega(m) = m+\Omega(n^{1.5})$ when the shortest cycle in the graph has a length of at least five. We complement this result with a simple randomized algorithm that synthesizes a graphic parity network with expected $m + O(n^{1.5}\sqrt{\log n})$ gates.

Additionally, we begin exploring connected graphs that allow for graphic parity networks with exactly $m + n - 1$ gates. We conjecture that all such graphs belong to a newly defined graph class. Furthermore, we present a linear-time algorithm for synthesizing minimum graphic parity networks for graphs within this class. However, this graph class is not closed under taking induced subgraphs, and we show that recognizing it is NP-complete, which is complemented with a fixed-parameter tractable algorithm parameterized by the treewidth.

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1 Introduction

Over the past decade, there has been significant progress in quantum computation, with advancements in both experimental and theoretical aspects [5, 16, 21, 7]. However, the technology remains constrained by the noise sensitivity of quantum hardware. Unlike classical logic, where circuit size largely dictates *efficiency*, in quantum circuits, size dictates *correctness*. In the current regime of Noisy Intermediate-Scale Quantum (NISQ) computing, where error correction remains prohibitively expensive, the fidelity of a quantum state decays exponentially with the number of gates. Consequently, even a constant-factor reduction in gate count—particularly for error-prone *two-qubit* gates—does not merely accelerate computation; it can be the deciding factor in whether a circuit yields a statistically distinguishable computational result or meaningless random noise. In the NISQ era, circuit optimization is not a luxury of efficiency, but a fundamental requirement for computational utility [19, 27, 15, 29]. This paper studies a problem that arises in optimizing a specific class of quantum circuits.

Subcircuits consisting only of CNOT and R_z gates appear in many quantum algorithms, such as quantum simulation [20], quantum approximate optimization algorithm (QAOA) [9], variational quantum eigensolver (VQE) [24], etc. To optimize such quantum circuits with massive $\{\text{CNOT}, R_z\}$-only components, a widely employed method is to independently resynthesize these components, and this problem has been extensively treated by *parity network synthesis* [1, 12]. Parity network is a CNOT-only quantum circuit. In a sense, CNOT gates can be viewed as the quantum analog of classical XOR gates.[1] A CNOT gate applied to qubit wires i and j, denoted by $\text{CNOT}(i, j)$, changes the value of wire j to $a \oplus b$, where $a, b \in \mathbb{F}_2$ are the values of wires i and j, respectively. Here, wire i is the *control wire*, and wire j is the *target wire*. A CNOT circuit is called a *parity network* for a set family S if every element of S appears in the circuit as a *term* at some intermediate point, and the final values of the wires are the same as the original input, denoted by $x_1, x_2, \ldots, x_n \in \mathbb{F}_2$ [1], and we say that a wire has the *term* $A = \{a_1, \ldots, a_{|A|}\}$ on it if the value of a wire evaluates to $x_{a_1} \oplus \cdots \oplus x_{a_{|A|}}$.

The set family S defines a hypergraph. In certain applications, it is actually a graph, namely all terms in S are two-element sets. For example, the maximum cut problem asks for a bipartition of the vertex set of a graph such that the number of edges between the two parts is maximized. The well-known quantum adiabatic algorithm (QAA) [10] and QAOA [9] use the following formulation to solve the maximum cut problem on a graph G:

$$\max_{x \in \{-1,1\}^{|V(G)|}} \sum_{(u,v) \in E(G)} \frac{1 - x_u x_v}{2}.$$

A principal component of the quantum circuit of these algorithms is a parity network with each term being a two-element set. A similar approach has been taken by many authors [28, 30, 31, 32, 4, 3, 2, 26], and there have been preliminary physical demonstrations of these quantum algorithms on NISQ devices [23, 14]. Recently, heuristic attempts have been made to synthesize small parity networks [1, 12, 8]. As far as we know, however, none of them is accompanied by analysis of performance. Such parity networks where all terms in S are two-element sets are called *graphic parity networks*, and see Figure 1 as examples. This paper is mainly concerned with the graphic parity network synthesis problem.

[1] To make our work accessible to a general audience, we will minimize the use of quantum computing jargon in the main text. Consequently, our definitions and explanations might seem imprecise to quantum experts. For a more detailed and rigorous treatment, please refer to Appendix A.

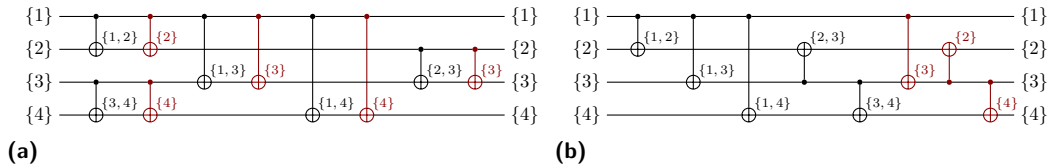


Figure 1 Two graphic parity networks for the graph with edges $\{\{1,2\},\{1,3\},\{1,4\},\{2,3\},\{3,4\}\}$, shown in Figure 2a. Each line represents a qubit wire labeled at the left. We use $i \bullet\!\!-\!\!\oplus\, j$ to denote $\textsc{cnot}(i,j)$. Indicated at the above right corner of $\oplus$ is the resulting term of this gate. The black terms correspond to the sets, and the red do not.

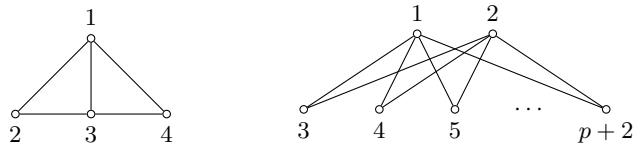


Figure 2 (a) A chordal graph, and (b) $K_{2,p}$, which can be made chordal by adding the edge $(1,2)$.

Our contributions The number of gates in a graphic parity network is called its *size*. Let G be the input graph, and let n and m denote the numbers of vertices and edges, respectively, in G. A trivial graphic parity network is in the fashion of Figure 1a; i.e., generating an edge and cleaning it up immediately. This leads to a trivial upper bound of $2m$, which is tight, as witnessed by graphs in which each component consists of one or two vertices. On the other hand, the definition implies a trivial lower bound, m, which, although tight, is uninteresting because it can only hold on edgeless graphs.

Our first result is a nontrivial lower bound of the size of graphic parity networks.

▶ **Theorem 1.** *A graphic parity network for a graph G contains at least $m + n - c$ gates, where c is the number of components of G.*

Again, this bound is tight: it matches the upper bound $2m$ for all forests. We say that a graphic parity network is *perfect* if its size is precisely $m + n - c$. A graph admits a graphic parity network that is perfect or close to perfect only when there are a lot of gates from two edge terms to another edge term, e.g., $\{1,3\} \oplus \{1,2\} = \{2,3\}$ in Figure 1b. The element 1 is canceled from the target wire of this gate, which is hence called a *cancellation*. A cancellation can only happen when the three edges form a triangle. As we will see, for *chordal graphs*—graphs in which every induced cycle is a triangle, it is easy to synthesize perfect graphic parity networks. This observation can be extended to graphs that can be turned into chordal graphs by adding a small number of edges, which contains many cycles of length three or four. See Figure 2 for examples. On the other hand, if the length of shortest cycles in a graph is five or more, we cannot do significantly better than the trivial construction of $2m$ gates.

▶ **Theorem 2.** *For any positive integer n, there exists a graph G with $\Omega\left(n\sqrt{n}\right)$ edges such that the size of its minimum graphic parity networks is $m + \Omega(m)$.*

Motivated by these observations, we propose a randomized algorithm for synthesizing graphic parity networks. It processes the vertices in a random order, and for each vertex v, generates all the edges between v and latter vertices. The algorithm tries to minimize the size by exploiting the triangles and squares in the input graph. The expected size of the

synthesized circuit almost matches the bound in Theorem 2. In particular, it produces very good results for dense graphs.

▶ **Theorem 3.** *There is a polynomial-time algorithm synthesizing a graphic parity network with expected size* $m + O\left(n^{1.5}\sqrt{\log n}\right)$*. Moreover, if all but a constant number of vertices have degrees* $\Omega(n)$*, the synthesized graphic parity network has expected size* $m + O\left(n \log n\right)$*.*

A natural question is to characterize graphs admitting PERfect graphic PArity NEtworks, which we call *perpane*. An immediate consequence of Theorem 1 is that in a perfect graphic parity network, there always exists a wire that is not a target of any gate. We noticed that for all perpane graphs we have discovered, we can synthesize a perfect graphic parity network in which there exists a wire that is not a control of any gate, e.g., wires 2 and 4 in Figure 1b. All edges involving the vertex v corresponding to this wire have to be generated along it, and the removal of this wire leads to a reduced graphic parity network for the subgraph $G - v$. Thus, there must be precisely $d + 1$ gates targeting this wire, where d is the number of neighbors of v in G. Except for the first and the last, each gate on this wire makes a new edge term by cancellation. This motivates us to define *perfect cancellation orderings* and *perfect cancellation graphs*. The formal definition is technical and hence deferred to Section 2.2. All chordal graphs are perfect cancellation graphs: all perfect elimination orderings [25] are perfect cancellation orderings, but not the other way. As we will see, a perfect cancellation ordering can guide us in synthesizing a perfect graphic parity network for G in linear time.

▶ **Theorem 4.** *All perfect cancellation graphs are perpane. Given a perfect cancellation graph* G *and a perfect cancellation ordering of* G*, we can synthesize a perfect graphic parity network for* G *in linear time.*

We conjecture that the two graph classes are equivalent: a graph is perpane if and only if it is a perfect cancellation graph. We leave it to the reader to verify that a simple cycle on four vertices is not a perfect cancellation graph, while it becomes one after adding a universal vertex, i.e., a vertex that is adjacent to all the vertices on the cycle. Thus, the class of perfect cancellation graphs is not *hereditary*, i.e., closed under taking induced subgraphs. The same holds for perpane graphs. This suggests that both classes are not easy to handle algorithmically. Indeed, finding a perfect cancellation ordering is computationally hard.

▶ **Theorem 5.** *It is* NP*-complete to decide whether a graph is a perfect cancellation graph.*

Finally, we present a fixed-parameter tractable algorithm for recognizing perfect cancellation graphs, using the treewidth of the input graph as the parameter. Similar to most algorithms using a tree decomposition, we use dynamic programming bottom-up. The main challenge is that a subgraph may need vertices from outside to make a perfect cancellation ordering. As said, the class of perfect cancellation graphs is not hereditary.

▶ **Theorem 6.** *The recognition of perfect cancellation graphs is fixed-parameter tractable parameterized by the treewidth of the input graph.*

Other related work Two other important measures for quantum circuits or reversible circuits are the depth and the number of ancillae. The *depth* of a quantum circuit is the count of time steps needed to execute all the gates in the circuit in parallel; e.g., the first two gates in Figure 1a contribute one to the depth. An *ancilla bit* is a qubit whose input is the particular state $\{0\}$ and can be utilized as auxiliary space throughout the computation but must be recovered to $\{0\}$ at the end of computation. The circuit depth characterizes

the running time of a quantum circuit, while the number of ancillae characterizes the extra space required by a quantum circuit. Any n-qubit CNOT circuit can be represented by an invertible matrix $\mathbb{M} \in \mathbb{F}_2^{n\times n}$, and the synthesis of CNOT circuit is equivalent to transforming $\mathbb{M}$ to identity by Gaussian elimination; see more details in the appendix. The main trick in minimizing circuit depth is to employ more ancillary qubits to eliminate multi-columns rather than one-column simultaneously [15, 18, 13]. Interestingly, this ultimately reduced to the parallel Gaussian elimination, which is inherently related to chordal graphs, also known as perfect elimination graphs. It is easy to see that any parity network for a connected graph has depth $\Omega(\log n)$. In fact, there is a trivial method synthesizing parity network for any graph in depth $O(\log n)$, as long as enough ancillae are given. This line of work is orthogonal to ours because it usually increases the size.

2 Graphic parity networks and perpane graphs

All graphs discussed in this paper are finite and simple. The vertex set and edge set of graph G are denoted by, respectively, $V(G)$ and $E(G)$. Throughout the paper we use $n = |V(G)|$ and $m = |E(G)|$. An n-qubit circuit over CNOT gates is a *graphic parity network* for a graph G if for every edge (u, v) of G, the term $\{u, v\}$ appears in the annotated circuit and the final state of the wires is the same as the original state.

A term is *singleton* or *binary* if its cardinality is one or two, respectively. For our purpose, this definition suffices, and we refer to Appendix A for a definition requiring more quantum background.

We start with proving lower bounds announced in Theorems 1 and 2. These proofs have two implications. First, we define a novel graph class that contains all chordal graphs, and show that all the graphs in this class admit the smallest possible graphic parity networks. Second, we propose a randomized algorithm for synthesizing graphic parity networks for general graphs.

2.1 Lower bounds

A parity network C can also be read from right to left, which defines another quantum circuit, called the *inverse* of C. Consider a wire with ℓ gates in C, which defines $\ell + 1$ terms. It turns out that the same wire in the inverse of C has the same number of terms, and they appear in exactly the reversed order as in C. This observation is formalized as the following proposition, which does not use any special properties of graphs and holds for all parity networks. For the sake of completeness, we provide a proof in Appendix B.

▶ **Proposition 7** (Folklore). *The inverse of a parity network for a set is a parity network for the same set. For each qubit wire, the wire in the inverse parity network has exactly the same terms, and they appear in the reversed order.*

The following bounds the number of non-binary terms generated by a graphic parity network.

▶ **Lemma 8.** *In any graphic parity network for a connected graph G, there must be at least $n - 1$ gates whose outcomes are not binary.*

Proof. Let ℓ be the size of the graphic parity network. For $i = 0, 1, \ldots, \ell$, we define a hypergraph H_i whose vertex set is $V(G)$ and whose edge set consists of all terms generated by the first i gates, and let $c(H_i)$ denote the number of components of H_i. By definition,

$$n = c(H_0) \geq c(H_1) \geq \cdots \geq c(H_\ell) = 1,$$

where $c(H_0) = n$ because H_0 is edgeless and $c(H_\ell) = 1$ because G is connected by assumption. In particular, $c(H_i)$ is either $c(H_{i-1})$ or $c(H_{i-1}) - 1$, and the second case can only happen when the ith gate is applied to two terms that are disjoint. Such a gate is called a plus-gate, and by the discussion above, there are at least $n - 1$ plus-gates.

We take the first $n - 1$ plus-gates of the graphic parity network, and denote them as $C_1, C_2, \ldots C_{n-1}$. For $i = 1, \ldots, n - 1$, we select a distinct gate of which the term on the target wire *before* the gate is non-binary. We take C_i if it satisfies our condition; otherwise, we take the next non-plus gate C'_i with the same target wire as C_i. Note that it exist because the final state of this wire is singleton. Since the term on the target wire is binary before C_i, and all gates between C_i and C'_i are plus-gates, the term on the target wire before C'_i is non-binary. All the $n - 1$ selected gates are distinct by the selection. In the inverse of this graphic parity network, these $n - 1$ non-binary terms appear *after* the gates, namely, there are $n - 1$ gates generating non-binary terms. And by Proposition 7, if a term is generated in the inverse, then it must be generated in the origin, and this concludes the proof. ◀

Theorem 1 is an immediate corollary of Lemma 8, and details are provided in Appendix C.

We say that a graphic parity network is *perfect* if its size is precisely $m + n - c$. A graph is called *perpane* if it admits a PERfect graphic PArity NEtwork.

By Lemma 8, there is a one-to-one mapping between $E(G)$ and the binary terms of a perfect graphic parity network. Moreover, if $m \gg n$, most of the terms for edges in G are generated by cancellation. Indeed, all chordal graphs admit perfect graphic parity networks. This can be extended to graphs close to chordal, e.g., the graph in Figure 2b, where $p = n - 2$. This graph can be turned into a chordal graph by adding a single edge, namely, $(1, 2)$, and hence it admits a graphic parity network of size $m + n = 3p + 2$. Note that all the induced cycles in $K_{2,p}$ have length four. If the girth of a graph is greater than four, the bound in Theorem 1 can be greatly improved.

▶ **Lemma 9.** *Let G be a graph of girth at least five. The minimum size of graphic parity networks for G is $m + \Omega(m)$.*

Proof. Let us fix a graphic parity network for G. For each edge $e \in E(G)$, let $f(e)$ denote the gate that generates the term corresponding to e, and $c(e)$ the immediately next gate targeting the same wire as $f(e)$; note that $c(e)$ exists because the final state of this wire is a singleton term. Let $F = \{f(e) \mid e \in E(G)\}$ and $C = \{c(e) \mid e \in E(G)\}$. Moreover, let R denote all the gates not in F. Note that $|F| = |C| = m$, and the size of the network is

$$|F| + |R| \geq |F| + |C \setminus F| = |F| + |C| - |F \cap C| = 2m - |F \cap C|.$$

We are done if $|F \cap C| \leq m/2$. Hence, we assume that $|F \cap C| > m/2$. By definition, each gate in $F \cap C$ is $c(e_1) = f(e_2)$ for two different edges e_1 and e_2. There are two cases,

$$\begin{cases} \{v, w\} \bullet\!\!-\!\!\oplus \{u, v\} & e_1 = (u, v), e_2 = (u, w), \\ \{u, v, w, x\} \bullet\!\!-\!\!\oplus \{u, v\} & e_1 = (u, v), e_2 = (w, x), \end{cases}$$

where the three or four vertices involved in the gate are all distinct. We use F_1 and F_2 to denote the sets of these two types of gates. Note that $F \cap C = F_1 \cup F_2$.

Case 1. Since G does not contain any triangles, (v, w) is not an edge. In other words, (v, w) is generated by a gate in R. Moreover, if there is another gate $c(e'_1) = f(e'_2)$ in F_1 using (v, w), then $e'_1 = (x, v)$ and $e'_2 = (x, w)$ for some vertex $x \neq u$. But then $uvxw$ is a cycle of length four, violating the assumption. Therefore, each gate in F_1 corresponds to a distinct gate in R.

Case 2. The term $\{u, v, w, x\}$ is generated by a gate in R. There are at most three gates in F_2 using the term $\{u, v, w, x\}$. Therefore, there are at least $|F_2|/3$ such 4-terms generated by R.

In summary, $|R| \geq |F_1| + \frac{|F_2|}{3} \geq \frac{|F_1|+|F_2|}{3} = \frac{|F \cap C|}{3} > \frac{m}{6}$. This concludes the proof. ◀

One missing element for proving Theorem 2 is the existence of large-girth dense graphs.

▶ **Theorem 10** (Restated from [11, Thm 4.5]). *For any positive integer n, there exists a graph G that has $\Omega(n\sqrt{n})$ edges and whose girth is at least five.*

In Appendix D we give a self-contained proof of Theorem 10 that constructs such graphs explicitly. We now use this result to complete the proof of our main result.

Proof of Theorem 2. By Theorem 10, there exists a graph G with n vertices and $m = \Omega(n\sqrt{n})$ edges whose girth is at least five. By Lemma 9, the size of its minimum graphic parity networks is $m + \Omega(m)$ which is $m + \Omega(n\sqrt{n})$. ◀

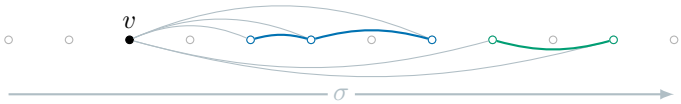
2.2 Perfect cancellation graphs

Let $N(v)$ denote the neighborhood of v, and $N(U) = \bigcup_{v \in U} N(v) \backslash U$ for a vertex set $U \subseteq V(G)$. Let $\sigma : V(G) \mapsto [n]$ be an ordering of the vertices of G, where $[n] = \{1, 2, \ldots, n\}$. A subset $U \subseteq V(G)$ is *σ-linked* if every two consecutive vertices in $\sigma|_U$, the sub-ordering of σ induced by U, are adjacent in G. We use $x <_\sigma y$ (resp., $x \leq_\sigma y$) to denote $\sigma(x) < \sigma(y)$ (resp., $\sigma(x) \leq \sigma(y)$). For each vertex $v \in V(G)$, we denote

$$N^+_\sigma(v) = \{u \in N(v) \mid \sigma(u) > \sigma(v)\}.$$

▶ **Definition 11.** *An ordering $\sigma : V(G) \mapsto [n]$ is a* perfect cancellation ordering *of G if for all vertices $v \in V(G)$ and for all components C of $G - v$, the set $N^+_\sigma(v) \cap C$ is σ-linked. A graph G is a* perfect cancellation graph *if it has a perfect cancellation ordering.*

The diagram below illustrates the situation for a vertex v in a perfect cancellation ordering σ. Note that for simplicity all irrelevant edges are hidden. In this diagram, there are two components in $G - v$. The neighbors of v in the blue component form a σ-linked set, as do those in the green component.



The vertex set of a chordal graph can be ordered such that, each vertex v and its neighbors that occur after v in the ordering form a clique; such an ordering is called a *perfect elimination ordering* [25]. Since a clique is σ-linked for any ordering σ, a perfect elimination ordering is a perfect cancellation ordering [25]. In other words, all chordal graphs are perfect cancellation graphs. It is worth noting that a perfect cancellation ordering of a chordal graph is not necessarily a perfect elimination ordering. For example, for the graph shown in Figure 2a, both $\sigma_1 = (1, 2, 3, 4)$ and $\sigma_2 = (4, 3, 2, 1)$ are perfect cancellation orderings, but only the second is a perfect elimination ordering because in the first ordering $N^+_{\sigma_1}(1) = \{2, 3, 4\}$ is a path instead of a clique. With a perfect cancellation ordering of G given, we can synthesize a perfect graphic parity network for G in linear time. Indeed, the circuit in Figure 1b was generated by Algorithm 1. For the convenience of presentation, we may start with biconnected graphs, for which the condition is simplified to $N^+_\sigma(v)$ being σ-linked for all v.

Algorithm 1 A synthesizing algorithm for perfect cancellation graphs

```
1  for i ← 2, 3, ..., n do                          ▷ [v_1, ..., v_n] is a perfect cancellation ordering of G
2  |  for j ← i − 1, i − 2, ..., 1 do
3  |  |  if (v_i, v_j) ∈ E(G) then                  ▷ j ∈ term(j) and |term(j)| ≤ 2
4  |  |  |  if term(j) = {j} then
5  |  |  |  |  CNOT(i, j);
6  |  |  |  else
7  |  |  |  |  {j, k} ← term(j);                   ▷ k > j and term(k) = {i, k}
8  |  |  |  |  CNOT(k, j);
9  for i ← n − 1, n − 2, ..., 1 do
10 |  {i, j} ← term(i);                            ▷ j > i and term(j) = {j}
11 |  CNOT(j, i);
```

▶ **Lemma 12.** *Let G be a biconnected graph. Given a perfect cancellation ordering of a graph G, we can synthesize a perfect graphic parity network for G in $O(m+n)$ time.*

Proof. Let σ be the perfect cancellation ordering. We may number the vertices such that $\sigma(v_i) = i$, and use Algorithm 1. It generates all the binary terms in the main loop (lines 1–8) before restoring the singleton terms in line 9. Initially, $\mathrm{term}(j) = \{j\}$ for all $j = 1, \ldots, n$. The algorithm maintains the following invariants. Before the execution of the ith iteration, for all $j = 1, \ldots, n$,

(I1) $j \in \mathrm{term}(j)$ and $|\mathrm{term}(j)| \leq 2$;

(I2) $\mathrm{term}(j) = \{j\}$ if $j \geq i$; and

(I3) if $\mathrm{term}(j) = \{j, k\}$, then $j < k < i$, $(v_j, v_k) \in E(G)$, and $(v_j, v_{k'}) \notin E(G)$ for all k' with $k < k' < i$.

Now we show that the invariants are maintained. In the iteration from the inner loop (lines 2 to 8), only $\mathrm{term}(j)$ is modified. By invariant I2, $\mathrm{term}(i) = \{i\}$, and it remains true during the ith iteration of the main loop because wire i is never the target. Moreover, for each $j < i$, wire j is the target in and only in the jth iteration of the inner loop. If $(v_i, v_j) \notin E(G)$, then $\mathrm{term}(j)$ is not changed, and all the invariants remain true. Hence, assume $(v_i, v_j) \in E(G)$, and we argue that $\mathrm{term}(j) = \{i, j\}$ after this iteration, and then all invariants remain satisfied afterward. It is straightforward when $\mathrm{term}(j) = \{j\}$ (line 5), and we focus on the else branch (line 6). Line 7 is correct by I1 and the fact that the condition in line 4 is not satisfied. By invariant I3, $k > j$, and $(v_{k'}, v_j) \notin E(G)$ for all k' with $k < k' < i$. Since σ is a perfect cancellation ordering, k and i are adjacent. By invariant I3, $\mathrm{term}(k) = \{k, i\}$, and thus line 8 sets $\mathrm{term}(j)$ to $\{k, i\}$. Thus, the algorithm correctly produces a graphic parity network for G.

We now verify that the synthesized circuit is perfect. For each edge, the algorithm introduces precisely one gate. Moreover, since G is connected, by invariant I3, $|\mathrm{term}(j)| = 2$ for all $j = 1, \ldots, n-1$ when the algorithm reaches line 9. By invariants I1 and I3, we can restore every wire to be a singleton term by one gate. Thus, the total size is precisely $m+n-1$.

Let us briefly explain the implementation. We assume the graph is stored as adjacency lists. It is pedestrian to reconstruct the lists such that each list is sorted. Thus, the number of iterations of the loop of line 3 can be the number of neighbors of v. The total time is thus $O(m+n)$ ◀

If G is not biconnected, we synthesize a graphic parity network for G by independently handling its biconnected components, and then concatenating the resulting circuits.

▶ **Observation 13.** *If G_1, G_2 are perpane graphs with perfect parity networks C_1, C_2, and they share a common vertex v, then the vertex contraction of G_1, G_2 at v is perpane, with a perfect parity network constructed by simply concatenating C_1 and C_2.*

The proof is straightforward: $|C_1 \cup C_2| = |C_1| + |C_2| = |V_1| + |E_1| - 1 + |V_2| + |E_2| - 1 = |V_1 \cup V_2| + |E_1 \cup E_2| - 1 = |V| + |E| - 1$.

▶ **Observation 14.** *Given a perfect cancellation ordering σ of a graph G and a biconnected component G_i of G, then $\sigma' := \sigma|_{V(G_i)}$ is a perfect cancellation ordering of G_i.*

Then Theorem 4 is a direct corollary of Lemma 12, Observation 13 and Observation 14.

2.3 A randomized synthesizing algorithm

Let G be an arbitrary graph. We present a randomized algorithm to synthesize a graphic parity network for G. We process the vertices in a random order, and for each vertex i, we generate all the edges between this vertex and latter vertices in this order, before resetting this wire to $\{i\}$. Similar to Algorithm 1, we never introduce a term with more than two elements, and the item i never leaves wire i. It has three phases.

The first phase only applies when the term on wire i is binary, i.e., it has an earlier neighbor in the order. Let j be the other number in this term. For all unprocessed neighbors v_k of v_i, if the term on wire k is $\{j, k\}$, we can generate $\{i, k\}$ by adding $\{i, j\}$ to it. The three vertices form a triangle.

In the second phase, we deal with neighbors v_j of v_i such that the term on wire j is binary. We group them according to the other item in their terms, and process each group by cancellation. Here we attempt to add a non-edge term $\{i, j\}$ to facilitate dealing with edges between v_i and common neighbors of v_i and v_j; see the discussion about $K_{2,p}$ above for motivation.

Finally, we deal with other neighbors of v_i individually. We summarize it as Algorithm 2.

Algorithm 2 A randomized algorithm for graphic parity network synthesis.

renumber the vertices such that $\pi(v_i) = i$; ▷ *π is a random permutation of $[n]$.*
for $i \leftarrow 1, 2, \ldots, n$ **do** ▷ *The size of each term is at most two.*
  if term(i) *is binary* **then**
    $\{i, j\} \leftarrow$ term(i); ▷ $j < i$.
    for $v_k \in N(v_i)$ ***such that*** term$(k) = \{j, k\}$ **do** ▷ $k > i$.
      CNOT(i, k);
      remove edge (v_i, v_k);
    CNOT(j, i);
  for $j \leftarrow 1, 2, \ldots, i-1$ **do**
    $K \leftarrow \{v_k \in N(v_i) \mid \text{term}(k) = \{j, k\}\}$;
    if $K \neq \emptyset$ **then** ▷ *$v_i v_j \notin E(G)$ or is already generated.*
      CNOT(j, i);
      for $v_k \in K$ **do** ▷ $k > i$.
        CNOT(i, k);
        remove edge (v_i, v_k);
      CNOT(j, i) ▷ *Clean up.*
  for $v_k \in N(v_i)$ **do** ▷ $k > i$.
    CNOT(i, k);
    remove edge (v_i, v_k);

We first prove the correctness of Algorithm 2. The algorithm starts with renumbering the vertices such that $\pi(v_i) = i$. Initially, $\text{term}(i) = \{i\}$ for all $i = 1, \ldots, n$. In the ith iteration of the main loop (lines 2–19), the algorithm generates all the terms for edges (v_i, v_k) with $k > i$, before resetting $\text{term}(i) = \{i\}$. If $\text{term}(i)$ is binary at the beginning, line 8 resets it. The only gates targeting wire i are lines 12 and 16. If line 12 changes wire i, line 16 duly resets it. It remains to verify that all edges are generated. Let v_k be a neighbor of v_i with $k > i$. If $\text{term}(k)$ is not binary before the ith main loop, it is added by either line 6 or line 15, depending upon whether $\text{term}(i)$ and $\text{term}(k)$ have an item. Thus, the algorithm correctly produces a graphic parity network for G. The algorithm clearly runs in polynomial time. In Algorithm 2, except for lines 12 and 16, each other gate either generates a new item or clears up a wire. Therefore, to bound the size of the synthesized circuit, it suffices to bound the number of them being executed. Since they are always executed in pair, it suffices to count line 12. For a set X, we use $\mathfrak{S}_X$ to denote the set of all permutations of X, and we use $\mathfrak{S}_n$ as a shorthand for $\mathfrak{S}_{[n]}$. The degree of vertex v is $d(v)$.

▶ **Lemma 15.** *The expected number of line 12 being executed is upper bounded by* $4n + \min_{1 \le t \le n} \left\{ 2\sum_{i<t} d_i + \frac{(n-t)n\log n}{d_t} \right\}$, *where* $d_1, d_2, \ldots, d_n$ *are the degrees of the vertices sorted in ascending order.*

Proof. Line 12 is only executed when $K \neq \emptyset$ and $i \notin \text{term}(j)$ at the beginning of the ith iteration. With permutation π, the number of line 12 being executed is the number of pairs (u, v) such that there exists an extra vertex w satisfying (i) $uw, vw \in E(G)$; (ii) u is not the last neighbor of v in π; (iii) $\pi(u) < \pi(v) < \pi(w)$; and (iv) $wx \notin E(G)$ for all vertices x with $\pi(u) < \pi(x) < \pi(v)$. Therefore, it cannot be more than the number of pairs (u, v) such that there exists an extra vertex w merely satisfying (iv) and (v) $uw, vw \in E(G)$ and $\pi(u) < \pi(v)$ (which is implied by (i-iii)). Now we upper bound the number of such pairs.

For any permutation $\pi \in \mathfrak{S}_n$, let $P(\pi)$ denote all such pairs when the algorithm is executed using permutation π, and let $P(\pi, j)$ denote the subset of $P(\pi)$ in which the first vertex is fixed by $\pi(u) = j$. Then the expected number of such pairs is

$$\begin{aligned}\mathop{\mathbb{E}}_{\pi\in\mathfrak{S}_n} |P(\pi)| &= \mathop{\mathbb{E}}_{\pi\in\mathfrak{S}_n} \sum_{j=1}^{n} |P(\pi, j)| = \sum_{j=1}^{n} \mathop{\mathbb{E}}_{\pi\in\mathfrak{S}_n} |P(\pi, j)| \\ &= \sum_{j=1}^{n} \mathop{\mathbb{E}}_{X\in\binom{[n]}{j}} \mathop{\mathbb{E}}_{\substack{\pi\in\mathfrak{S}_X \\ \forall x\in X.\pi(x)>n-j}} |P(\pi, n-j+1)| \le \sum_{j=1}^{n} \mathop{\mathbb{E}}_{\pi\in\mathfrak{S}_n} |P(\pi, 1)|.\end{aligned}$$

Therefore, it reduces to bounding the expected size of $P(\pi, 1)$. Consider any fixed $t \in [n]$. If $d(\pi^{-1}(1)) \le d_t$, then $|P(\pi, 1)| \le d_t$. We now consider the nontrivial case, where $d(\pi^{-1}(1)) > d_t$. Note that $|P(\pi, 1)|$ is the number of vertices v such that there exists another vertex w whose first two neighbors in π are $\pi^{-1}(1)$ and v; we say that it is *witnessed by* w. For each vertex $w \in N(\pi^{-1}(1))$, let X_w be the index of the second neighbor of x in π. Then

$$\mathbb{P}(X_w = i) = \left(1 - \frac{d(w)-1}{n-2}\right) \cdots \left(1 - \frac{d(w)-1}{n-(i-1)}\right) \frac{d(w)-1}{n-i} > \left(1 - \frac{d(w)-1}{n}\right)^{i-2} \frac{d(w)-1}{n}.$$

Letting $\alpha = 1 - \frac{d(w)-1}{n}$, we have

$$\begin{aligned}\mathbb{P}\left(X_w \le \frac{n\log n}{d(w)-1}\right) &= \mathbb{P}(X_w = 2) + \cdots + \mathbb{P}\left(X_w = \left\lfloor \frac{n\log n}{d(w)-1} \right\rfloor\right) \\ &> \frac{d(w)-1}{n} + \cdots + \alpha^{\left\lfloor \frac{n\log n}{d(w)-1} \right\rfloor - 2} \left(\frac{d(w)-1}{n}\right) = 1 - \alpha^{\left\lfloor \frac{n\log n}{d(w)-1} \right\rfloor - 1}.\end{aligned}$$

If $d(w) > d_t$, then $\frac{n\log n}{d(w)-1} \le \frac{n\log n}{d_t}$, and

$$\mathbb{P}\left(X_w > \frac{n\log n}{d_t}\right) < \alpha^{\left\lfloor \frac{n\log n}{d(w)-1}\right\rfloor - 1} = \left(1 - \frac{d(w)-1}{n}\right)^{\left\lfloor \frac{n\log n}{d(w)-1}\right\rfloor - 1} < \frac{4}{n}. \tag{1}$$

Since the number of such vertices w is less than $n-1$, then all such vertices witness at most $\frac{n\log n}{d_t} + 4$ vertices. On the other hand, each vertex w with $d(w) \le d_t$ witnesses at most one vertex. In summary, for each $u \in V(G)$,

$$\mathop{\mathbb{E}}_{\substack{\pi\in\mathfrak{S}_n \\ \pi(u)=1}} |P(\pi,1)| < \frac{n\log n}{d_t} + 4 + \sum_{\substack{w\in N(u) \\ d(w)\le d_t}} 1. \tag{2}$$

Combining the arguments above, we conclude that the expected number of line 12 being executed is less than

$$\sum_{d_i\le t} d_i + \sum_{\substack{u\in V(G) \\ d(u)>d_t}} \left(\frac{n\log n}{d_t} + 4 + \sum_{\substack{w\in N(u) \\ d(w)\le d_t}} 1\right) = 2\sum_{d_i\le t} d_i + \sum_{d_i>t} \frac{n\log n}{d_t} + 4n. \tag{3}$$

The statement follows because (3) holds for all $t \in [n]$. ◀

Theorem 3 is thus a direct consequence Lemma 15, whose proof is deferred to Appendix E.

3 Recognition of perfect cancellation graphs

For any graph class, the first algorithmic question is its *recognition*: to decide whether a given graph is in this class. In this section, we investigate the complexity and algorithms of recognizing perfect cancellation graphs.

3.1 The NP-completeness of recognition

We now prove Theorem 5 by a reduction from the following problem, which is shown to be NP-complete by Opatrny [22].

▶ **Definition 16** (Betweeness). *Given a finite set S and a set of ordered triples $T \subseteq S\times S\times S$, the betweenness problem asks to determine whether there exists a total ordering π of S such that for every triple (x,y,z) in T, either $x <_\pi y <_\pi z$ or $z <_\pi y <_\pi x$.*

The key observation of our reduction is to use a set of false twins to force the order on a triple of vertices with two edges among them. A set of vertices with the same neighborhood is called *false twins*. Note that by definition, there cannot be any edge among false twins.

▶ **Lemma 17.** *Let G be a perfect cancellation graph and I a set of false twins of G. If $|N(I)| \le |I| - 1$, then $N(I)$ is σ-linked in any perfect cancellation ordering σ of G,*

Proof. The statement holds vacuously if I comprises a single vertex. Hence, we assume that $|I| \ge 2$, and hence no vertex in I is a cut vertex. Let v be the first vertex in σ from $I \cup N(I)$. It suffices to show that $v \in I$: note that $N^+_\sigma(v) = N(v) = N(I)$. Suppose for contradiction that $v \notin I$, i.e., $v \in N(I)$. We may number the vertices in $N^+_\sigma(v)$ as $u_1,\dots,u_\ell$, where $\ell = |N^+_\sigma(v)|$, such that $u_i <_\sigma u_{i+1}$ for all $i = 1,\dots,\ell-1$. Since there is no edge among vertices in I, between any two of them there is another vertex, which has to be from $N(I)$. This is nevertheless impossible because there are at most $|N(I)\setminus\{v\}| \le |I| - 2$ such vertices. ◀

For example, in the Figure 3a, in any perfect cancellation ordering σ, either $v_1 <_\sigma v_2 <_\sigma v_3$ or $v_3 <_\sigma v_2 <_\sigma v_1$. We are now ready to describe the reduction from an instance (S, T) of the betweenness problem to the recognition of perfect cancellation graphs. Let $p = |S|$ and $q = |T|$. We construct a graph G on $2p+14q$ vertices as follows. First, for each element x in S, introduce a vertex; abusing notation, we use x to denote both the element and the corresponding vertex, and use S to denote this set of vertices. Second, we introduce a vertex set $C = \{v_1^i, v_3^i \mid 1 \le i \le q\}$. We add an edge between each pair of vertices in C unless they have the same superscript (note that the complement of the subgraph induced by C is an induced matching), and we add all the $2pq$ edges between S and C. Third, we add a set U of p vertices, and make them universal in the subgraph induced by $S \cup C \cup U$.

Finally, we add the sets of false twins to enforce the desired order. We use (v_0^i, v_2^i, v_4^i) to denote the three vertices in S corresponding to the three elements in the ith triple in T in order. For each $i = 1, \ldots, q$, we introduce 12 vertices $z_1^i, \ldots, z_{12}^i$. For each $j = 0, 1, 2$, let $Z_j^i = \{z_{4j+1}^i, \ldots, z_{4j+4}^i\}$, and add all the 12 edges between Z_j^i and $\{v_j^i, v_{j+1}^i, v_{j+2}^i\}$. See Figure 3b for an illustration.

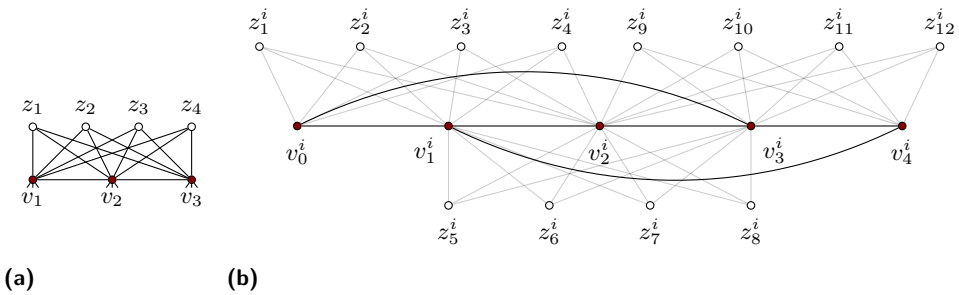


Figure 3 Demonstration for (a) Lemma 17 and (b) Theorem 5.

Proof of Theorem 5. It is easy to check whether an ordering is a perfect cancellation ordering, the recognition of perfect cancellation graphs is in NP. For its NP-hardness, we show that (S, T) is a yes-instance of the betweenness problem if and only if the graph G constructed above is a perfect cancellation graph.

For sufficiency, suppose that G is a perfect cancellation graph, and let $\sigma : V(G) \mapsto [2p+14q]$ be a perfect cancellation ordering of G. For $i = 1, \ldots, q$, Lemma 17 applied to the set Z_1^i forces that either $v_1^i <_\sigma v_2^i <_\sigma v_3^i$ or $v_3^i <_\sigma v_2^i <_\sigma v_1^i$. We may assume without loss of generality that $v_1^i <_\sigma v_2^i <_\sigma v_3^i$, and the other is symmetric. Then Lemma 17 applied to sets Z_0^i and Z_2^i forces that

$$v_0^i <_\sigma v_1^i <_\sigma v_2^i \text{ and } v_2^i <_\sigma v_3^i <_\sigma v_4^i,$$

Thus, $v_0^i <_\sigma v_2^i <_\sigma v_4^i$, and $\pi = \sigma|_S$ is a valid ordering of S that certificates that (S, T) is a yes-instance.

For necessity, suppose that (S, T) is a yes-instance of the betweenness problem, and let π be a valid ordering of S. We may number the elements in S such that $\pi = \langle x_1, \ldots, x_p \rangle$. Since reversing triples in T does not change the instance, we may assume without loss of generality that for all $i = 1, \ldots, q$, $v_0^i <_\pi v_2^i <_\pi v_4^i$. For $i = 1, \ldots, p$, let $c(i)$ denote the number such that $x_{c(i)} = v_2^i$; note that $1 < c(i) < p$. We number the vertices in U as $\{u_1, \ldots, u_p\}$.

We construct a perfect cancellation ordering σ of $V(G)$ as follows. It starts from

$$z_1^1, \ldots, z_{12}^1, \ldots, z_{12}^q, u_1, x_1, \ldots, u_p, x_p.$$

For all $i = 1, \ldots, q$, we put v_1^i in between $x_{c(i)-1}$ and $u_{c(i)}$ and v_3^i in between $x_{c(i)}$ and $u_{c(i)+1}$; vertices assigned to the same range are in an arbitrary order. Note that

$$\sigma(x_i) = 12q + 2i + 2|\{j \mid c(j) < i\}| + |\{j \mid c(j) = i\}|.$$

Now we verify that σ is a perfect cancellation ordering of G. By construction,

$$v_0^i \leq_\sigma x_{c(i)-1} <_\sigma v_1^i <_\sigma x_{c(i)} = v_2^i <_\sigma v_3^i <_\sigma x_{c(i)+1} \leq_\sigma v_4^i.$$

Thus, $N_\sigma^+(z_j^i) = N(z_j^i)$ is σ-linked for all $i = 1, \ldots, q$ and $j = 1, \ldots, 12$. If two vertices after z_{12}^q in σ are not adjacent, they are either x_j and x_i for $1 \leq j < i \leq q$, or v_1^i and v_3^i for some i. Such a pair is always separated by the vertex u_i. Since u_i is universal in the subgraph induced by $S \cup C \cup U$, the ordering σ is a perfect cancellation ordering of G. ◀

3.2 Recognition is fixed-parameter tractable

We give some intuitions of the algorithm and defer the details to Appendix F. During a bottom-up dynamic programming on a nice tree decomposition, we can partition the vertices into P, C, and F, which denotes the set of forgotten vertices, vertices in the current bag, and vertices not yet introduced, respectively. By definition, there is no edge between P and F. Thus, for a perfect cancellation ordering σ and any vertex v, the path on $\sigma|_{N_\sigma^+(v)}$ will be broken into several sub-paths with vertices in P removed, whose endpoints (except the original endpoints of the path) are all from C. Using this fact, we can then record the partially constructed orderings by recording the endpoints of the sub-paths for vertices in C.

4 Concluding remarks

The main open problem is whether all perpane graphs have perfect cancellation orderings.

▶ **Conjecture 18.** *A graph is perpane if and only if it is a perfect cancellation graph.*

We know that there are perfect graphic parity networks that do not correspond to any ordering in an apparent way. Thus, to answer the conjecture, we need to better understand perfect graphic parity networks, for which there are several open questions. In particular, whether a perpane graph always admits

(C1) a perfect graphic parity network in which all terms are singleton and binary;
(C2) a perfect graphic parity network in which some wire is not a control of any gate; and
(C3) a perfect graphic parity network in which no qubit leaves its original wire.

For all the properties, we have examples of perfect graphic parity networks violating them (see Appendix G). But we can find alternative perfect graphic parity networks with the desired properties. Note that Lemma 8 does not rule out the existence of terms of cardinality three or more, though it does imply that if there is such a term, there are more wires that remain singleton throughout.

If a graph contains a set U of $\lfloor \frac{n}{2} \rfloor$ universal vertices, then we can make a perfect cancellation ordering by arranging the vertices in $V(G) \setminus U$ and in U alternatively.

▶ **Proposition 19.** *A graph containing $\lfloor \frac{n}{2} \rfloor$ universal vertices is a perfect cancellation graph.*

An interesting question arising from Proposition 19 is: given a graph, what is the minimum number of universal vertices we need to add to make it a perfect cancellation graph? Even more interesting is adding edges. Since all chordal graphs are perfect cancellation graphs, this cannot be larger than the well-studied chordal completion number [6, 17]. Can we always turn a graph into a perfect cancellation graph by adding at most m edges? We would not bother if it needs more than m: any graph has a trivial graphic parity network of size $2m$.

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A More quantum background

Let $x, b \in \mathbb{F}_2^n$, then $x \cdot b = x_1 b_1 \oplus x_2 b_2 \oplus \cdots \oplus x_n b_n$.

▶ **Definition 20** ([AAM18]). *Given $S \subseteq \mathbb{F}_2^n$, a* parity network *for S is an n-qubit* CNOT *circuit that, with initial state $|b\rangle$,*

- *for all $x \in S$ the state $|x \cdot b\rangle$ appears on a certain qubit in the circuit; and*
- *the final state is $|b_1, b_2, \ldots, b_n\rangle$.*

The second requirement is from quantum algorithms like QAA and QAOA, where the original state must be restored at the end of the circuit. In applications like QAOA, the output is allowed to be a permutation of the input, i.e., the final state can be $\left|b_{\pi(1)}, b_{\pi(2)}, \ldots, b_{\pi(n)}\right\rangle$ for some permutation $\pi \in \mathfrak{S}_n$. But allowing this seems not only to fail to aid in resolving the problem but also to further complicate it, so our definition restricts the output to be exactly the same as the input.

We now briefly explain the use of graphic parity networks in optimizing the quantum circuits for QAA and QAOA. Recall the following formulation of the maximum cut problem:

$$\max_{x \in \{-1,1\}^{|V(G)|}} \sum_{(u,v) \in E(G)} \frac{1 - x_u x_v}{2}.$$

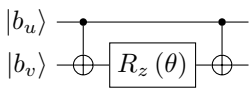
In the Ising formulation [Luc14], it is equivalent to finding the ground energy (lowest eigenvalue) of the following Hamiltonian:

$$H_C = \sum_{(u,v) \in E} Z_u Z_v,$$

where Z_u stands for the Pauli Z operator acting on the qubit u. Both QAA and QAOA use the quantum adiabatic evolution to calculate the ground energy of H_C as follows.

1. Select a Hamiltonian H_B such that H_B has a simple ground state.
2. Initialize the quantum state to the ground state of H_B.
3. Evolve the quantum state under a time-dependent Hamiltonian that gradually changes from H_B to H_C.
4. The final state of the quantum system is the ground state of H_C, whose energy can be measured to obtain the solution to the maximum cut problem.

In the quantum circuit model, for the evolving of quantum state under a gradually changing Hamiltonian, one common approach is Trotter–Suzuki decomposition [Suz91], where $\exp(iH_B\theta)$ and $\exp(iH_C\theta)$ should be implemented. For the implementation of $\exp(iH_C\theta)$, the parity networks come into play. For example, the naive implementation of $\exp(iH_C\theta)$ can be done by applying the following sequence of gates for all $(u, v) \in E(G)$:



where R_z is the single qubit gate rotating along Pauli-Z axis. Suppose the input for the circuit is $|b_u, b_v\rangle$, then the output will be $\exp(-i(b_u \oplus b_v)\theta)|b_u, b_v\rangle$, which is the desired effect of $\exp(iH_C\theta)$. So suppose we have a parity network with a small size, we can implement the operation $\exp(iH_C\theta)$ by appropriately inserting R_z gates where a new binary term is generated. See Figure 4 for an example of how the parity network in Figure 1b can be transformed into a circuit implementing $\exp(iH_C\theta)$.

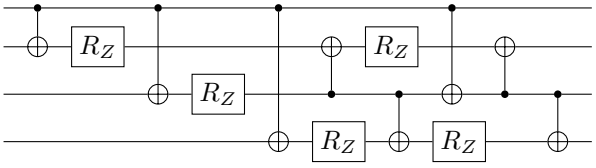


Figure 4 The corresponding circuit of the parity network in Figure 1b. It is generated by inserting a R_z gate whenever and wherever a new parity term is generated.

A CNOT gate can also be represented as an invertible matrix over $\mathbb{F}_2^{n\times n}$, i.e.,

$$\text{CNOT}(i,j) = \begin{pmatrix} 1 & & & & & & \\ & \ddots & & & & & \\ & & 1 & & & & \\ & & & \ddots & & & \\ & & 1 & & 1 & & \\ & & & & & \ddots & \\ & & & & & & 1 \end{pmatrix}.$$

Thus, the transformation applied by an n-qubit CNOT circuit can be written as an invertible matrix $\mathbb{M} \in \mathbb{F}_2^{n\times n}$, and the optimization of CNOT circuits is equivalent to transforming $\mathbb{M}$ to identity using row-addition operations, and each row-addition actually corresponds to a CNOT gate. Therefore, the optimization of CNOT circuit is equivalent to minimizing the number of row-additions to transform an invertible matrix to identity.

B Proof of Proposition 7

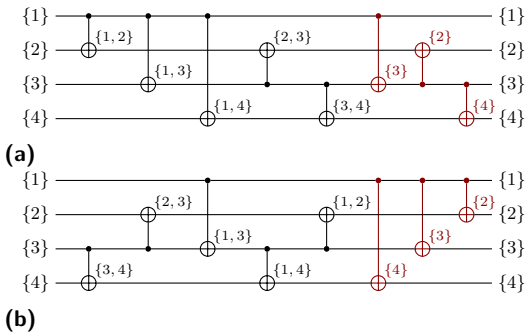


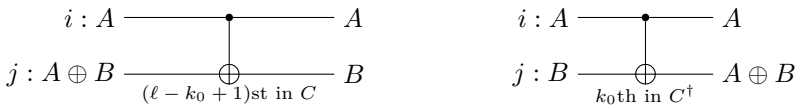
Figure 5 (a) The parity network Figure 1b and (b) its inverse.

We prove by induction on the number of gates executed in the circuit. To be precise, given a parity network C of ℓ gates and its inverse $C^\dagger$, for all $k = 0, 1, 2, \ldots, \ell$, we prove that if we execute the first k gates in $C^\dagger$ and the first $\ell - k$ gates in C, the terms on wire i in C will be the same as the term on wire i in $C^\dagger$.

Base case: When $k = 0$, the statement is trivially true, since the C has finished with the term on wire i in C being $\{i\}$, and $C^\dagger$ has not started yet with the term on wire i being $\{i\}$.

Inductive step: Suppose the statement is true for $k = 0, 1, \ldots, k_0 - 1$. We suppose the $(\ell - k_0)$-th gate in C is $\text{CNOT}(i, j)$ and thus makes the k_0-th gate in $C^\dagger$ be $\text{CNOT}(i, j)$. By

the induction hypothesis, the terms on wire i in C and i in $C^\dagger$ are the same, and we denote them by A. Likewise, we use B to denote the term on j. So after the k_0-th gate, the wire j in $C^\dagger$ evaluates to $A \oplus B$, the same as the term on wire j before the $(\ell - k_0 + 1)$-th gate in C. Therefore, the statement is true for k_0 and the induction is complete.



By the induction, every term generated in C has also been generated in $C^\dagger$ (and vice versa) and Proposition 7 is proved.

C Proof of Theorem 1

Proof of Theorem 1. We do induction on the number of components c of G. If $c = 1$, the claim follows directly from Lemma 8, since there are m gates generating binary terms and at least $n - 1$ generating non-binary terms, summing to at least $m + n - 1$ gates. Now, assume that the claim holds for all graphs with up to $c - 1$ components, and let G be a graph with c components. Given a graphic parity network C for G, we gather all ≥ 2 terms generated by C, and let c' be the number of components formed by the hypergraph consisting of these terms. Note that $1 \leq c' \leq c$. Suppose $c' < c$, then by inductive hypothesis, $|C| \geq m + n - c' > m + n - c$. Otherwise, this parity network can be seen as the union of c independent graphic parity networks, so the number of gates that generates non-binary terms is at least $\sum_{i=1}^{c}(n_i - 1) = n - c$, where n_i is the number of vertices in the i-th component. Therefore, $|C| \geq m + n - c$. This concludes the proof. ◀

D Proof of Theorem 10

For an integer $k \geq 2$, a *finite projective plane* of order k is a plane with $k^2 + k + 1$ points and $k^2 + k + 1$ lines such that

(P1) $k + 1$ points on each line;
(P2) $k + 1$ lines through each point;
(P3) for any two distinct points, there is a unique line passing through them; and
(P4) for any two distinct lines, there is a unique point on both lines.

▶ **Theorem 21** ([Kár76]). *For each a prime power k, there exists a finite projective plane of order k.*

We give the following lemma which is used in our construction, whose proof is deferred to the end of this section.

▶ **Lemma 22.** *For any $t \geq 21$, the largest prime number p satisfying*

$$p^2 + p + 1 \leq t \tag{4}$$

also satisfies

$$p^2 + p + 1 > \frac{t}{4}.$$

We construct a bipartite graph out of a finite projective plane as follows; see Figure 6 for an illustration.

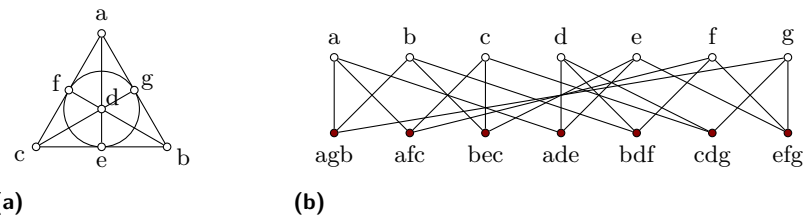


Figure 6 (a) The Fano plane, a finite projective plane of order 2, and (b) the bipartite graph constructed.

Proof. For arbitrary $n \geq 42$, we take k to be the largest prime power such that $k^2+k+1 \leq n/2$, and take a finite projective plane of order k. We construct a graph G as follows. For each point p and each line ℓ in the projective plane, we introduce a vertex, denoted by u_p and v_ℓ, respectively. We add an edge between u_p and v_ℓ if and only if p is on ℓ. Finally, we add $n - 2(k^2 + k + 1)$ isolated vertices to make n vertices in total. By (P1), (P2) and Lemma 22, $m = (k^2 + k + 1)(k + 1) = \Theta\left(n\sqrt{n}\right)$. The graph cannot contain any triangle because every edge is between a point vertex and a line vertex; moreover, by (P3) and (P4), there cannot be an induced cycle on four vertices. Thus, the girth of G is at least five. ◀

Finally, to prove Lemma 22, we restate a classical result from elementary number theory:

▶ **Theorem 23** (Bertrand's Postulate [Che52]). *For any integer $n > 1$, there exists a prime p such that $n < p < 2n$.*

The proof of Lemma 22 proceeds as follows:

Proof. Let x be the largest positive integer satisfying $x^2 + x + 1 \leq t$. When $t \geq 21$, x must exist and $x \geq 4$. This implies $\left\lceil \frac{x}{2} \right\rceil \geq 2$. By Theorem 23, there exists a prime q such that

$$\left\lceil \frac{x}{2} \right\rceil < q < 2\left\lceil \frac{x}{2} \right\rceil \leq x + 1,$$

i.e.,

$$\left\lceil \frac{x}{2} \right\rceil < q \leq x.$$

Since p is the largest prime satisfying (4),

$$p \geq q > \left\lceil \frac{x}{2} \right\rceil,$$

which yields

$$p^2 + p + 1 \geq \left\lceil \frac{x}{2} \right\rceil^2 + \left\lceil \frac{x}{2} \right\rceil + 1 > \frac{t}{4}.$$

◀

Finally, Theorem 4 is a direct consequence of Lemma 12, Observation 13 and Observation 14, since all cut vertices and biconnected components can be obtained in linear time [JR73].

E Proof of Theorem 3

Proof of Theorem 3. We have seen Algorithm 2 always correctly synthesizes a graphic parity network. We now analyze its expected size. Each gate in lines 6, 14, and 18 generates a term for a new edge. Thus, the total number of them is m. Line 8 is executed at most once for each vertex, and hence the total number is at most n. Let s_{12} denote the expected number of executions of line 12. Therefore, the expected circuit size synthesized by this algorithm is at most $m + 2s_{12} + n$, which is $m + O(n^{1.5}\sqrt{2\log n})$ because

$$\min_{1\le t\le n}\left\{2\sum_{i<t} d_i + \frac{(n-t)n\log n}{d_t}\right\} \le \min_{1\le t\le n}\left\{2td_t + \frac{(n-t)n\log n}{d_t}\right\}$$
$$\le \min_{d}\left\{2nd + \frac{n^2\log n}{d}\right\} = n^{1.5}\sqrt{2\log n}.$$

Moreover, when all but a constant number c_1 of vertices have degrees at least $c_2 n$, we have

$$\min_{1\le t\le n}\left\{2\sum_{i<t} d_i + \frac{(n-t)n\log n}{d_t}\right\} \le 2\sum_{d_i<c_2 n} d_i + \frac{(n-c_1)n\log n}{c_2 n} \le 2c_1c_2 n + \frac{1}{c_2} n\log n.$$

Thus, the size is $m + O(n\log n)$. ◀

F Sketch of the parameterized algorithm

First we give the definition of nice tree decomposition. A tree decomposition $\mathcal{T} = (T, \{X_t\}_{t\in V(T)})$ is *nice* if it satisfies the following properties:

- $X_r = \emptyset$ and $X_\ell = \emptyset$ for every leaf ℓ of T. In other words, all the leaves as well as the root contain empty bags.
- Every non-leaf node of T is of one of the following three types:
  - Introduce node: a node t with exactly one child t' such that $X_t = X_{t'} \cup \{v\}$ for some vertex $v \notin X_{t'}$; we say that v is *introduced* at t.
  - Forget node: a node t with exactly one child t' such that $X_t = X_{t'} \setminus \{v\}$ for some vertex $v \in X_{t'}$; we say that v is *forgotten* at t.
  - Join node: a node t with two children t_1, t_2 such that $X_t = X_{t_1} = X_{t_2}$.

For each node, we will keep track of all the valid orderings, defined below. Let V_t be the set of vertices that are introduced in the subtree rooted at t, and without loss of generality we assume the input is bi-connected.

▶ **Definition 24.** *Let t be a node of T. A permutation σ of V_t is valid for t if*

(V1) *for each $v \in V_t \setminus X_t$, the set $N^+_\sigma(v)$ is σ-linked; and*

(V2) *for each $v \in X_t$, if two consecutive vertices in $\sigma|_{N^+_\sigma(v)}$ are not adjacent, they must be in X_t.*

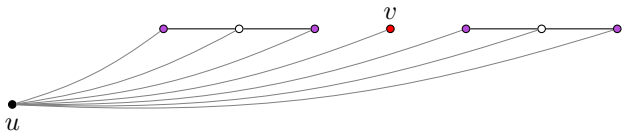
Now we introduce the definition of canonical representation which helps us to compress the space of valid orderings. For a node $t \in V(T)$ and a permutation σ of V_t and a vertex $v \in X_t$, the *canonical representation* of $\sigma|_{N^+_\sigma(v)}$ of σ under X_t is an ordered set of endpoints $\{(p_1, q_1), (p_2, q_2), \ldots, (p_k, q_k)\}$ such that for all i,

1. $p_i, q_i \in X_t \cup \{\dashv, \vdash\}$, only p_1 is allowed to be $\dashv$, only q_k is allowed to be $\vdash$,
2. segments do not intersect, i.e., $\sigma(q_i) < \sigma(p_{i+1})$,
3. the subset of elements in $N^+_\sigma(v)$ covered by this segment, i.e., $C_i = \{v \mid v \in N^+_\sigma(v) \wedge \sigma(p_i) \le \sigma(v) \le \sigma(q_i)\}$, is σ-linked,

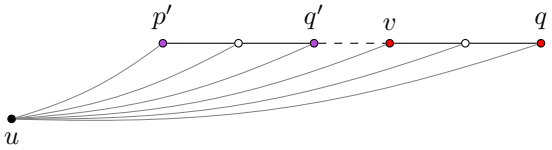
4. there are no two consecutive X_t elements in $\sigma|_{C_i}$, and
5. all segments together cover all $N^+_\sigma(v)$, i.e., $\bigcup_{i=1}^{k} C_i \setminus \{\dashv, \vdash\} = N^+_\sigma(v)$.

In our algorithm, we will keep track of all canonical representations of $\sigma|_{N^+_\sigma(v)}$ for $v \in X_t$. To be precise, for each node $t \in V(T)$, we will construct a set c_t that consists of all pairs (τ, b) describing a valid ordering σ such that:
(V1) τ is the restriction of σ to X_t, and
(V2) for each v in the current bag, b_v is the canonical representation of $\sigma|_{N^+_\sigma(v)}$ under X_t.
Now we discuss how c_t can be constructed in a bottom-up manner, and finally the graph is a perfect cancellation graph if and only if for the root bag r, $c_r \neq \emptyset$. For leaf nodes, the construction is trivial.

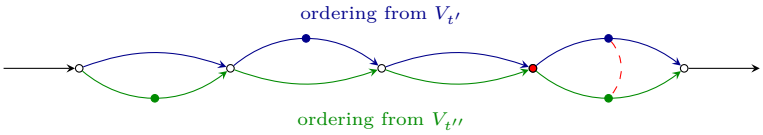
For an introduce node t with child t' such that $X_t = X_{t'} \cup \{v\}$ for some v, we process all canonical representations τ', b' in c'_t. We enumerate the position in τ' after which v is being inserted, and for a vertex $u \in N(v)$ that precedes v, its set of succeeding neighbors will also add v. Then we check whether v is being placed between two segments in b'_u since only the endpoints of the segments are allowed to have new neighbors, and if all checks pass, we can construct b_u by inserting (v, v) to the appropriate position in b'_u.



For a forget node t with child t' such that $X_t = X_{t'} \setminus \{v\}$ for some v, we process all canonical representations τ', b' in c'_t. We first check whether the succeeding neighbors of v are connected, and if not, since no new neighbors of v will be introduced, $N^+_\sigma(v)$ will never become σ-linked, we skip this τ', b'. Then we construct τ, b by deleting v from τ' and b'. For each $u \in N(v)$ that lies in the front of v, we check if v can be deleted safely from its succeeding neighbors. Without loss of generality, we assume there is a segment (v, q) in b'_u, and the predecessor of (v, q) is (p', q'), then we check whether q' is connected to v (the dashed edge must exist), because if not, after v is forgotten, q' can never be connected to v so $N^+_\sigma(u)$ can never be σ-linked. If the check passes, we should replace the segments $(p', q'), (v, q)$ with a single (p', q), and b_u is constructed.



For a join node t with children t', t'', then two valid orders in the two subtrees $V_{t'}$ and $V_{t''}$ can be merged only if between any pair of adjacent X_t vertices in the order, either all vertices are from $V_{t'}$ or all vertices are from $V_{t''}$, otherwise the endpoint after which clash occurs (indicated red below) will not have a σ-linked succeeding neighborhood. On the other hand, once the condition holds, the full ordering can be constructed by arbitrarily merging the two orderings, and b_u can be constructed by simply merging b'_u and b''_u as well.



G Examples of perfect graphic parity networks violating the conditions

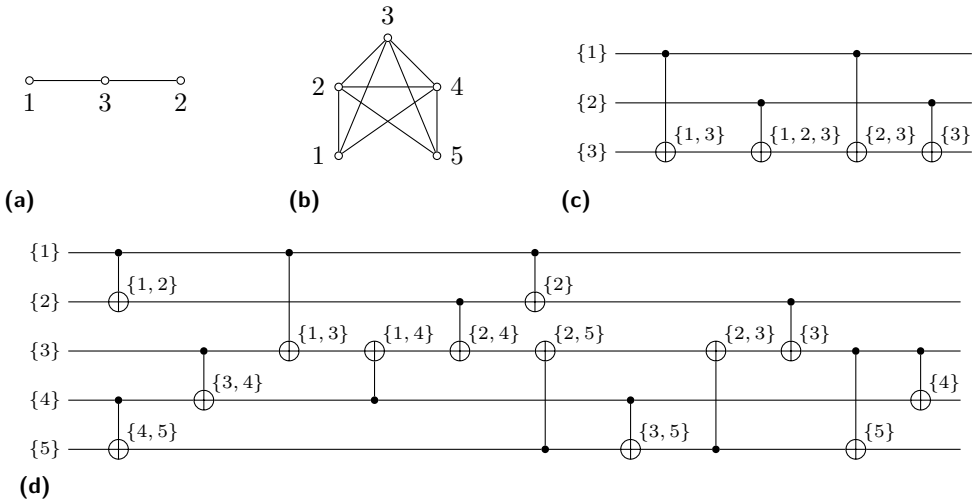


Figure 7 Perfect graphic parity networks that do not satisfy the conditions. (a) A line of length 3. (b) A chordal graph. (c) A perfect graphic parity network for (a) violating C1. (d) A perfect graphic parity network for (b) violating C2, C3.

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